

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Douglas A. Larson and Attorney Docket No.: 501296.01 (30266/US)
Jeffrey J. Cronin
Filed : Concurrently Herewith
Title : APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL
DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

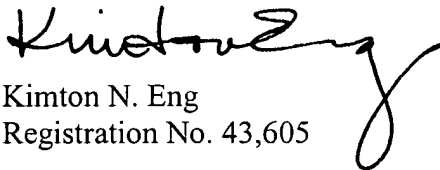
Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicants wish to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. Copies of the non-patent literature references, as required under 37 C.F.R. § 1.98(a)(2), are enclosed. Copies of the cited U.S. patents and U.S. patent application publications will not be submitted herewith in accordance with the waiver by the Office of the requirement under 37 C.F.R. § 1.98(a)(2)(i) for U.S. national patent applications filed after June 30, 2003. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP


Kimton N. Eng
Registration No. 43,605

KNE:ajs

Enclosures:

Postcard
Form PTO-1449
Cited References (2)

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FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501296.01 (30266/US)	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>		APPLICANT(S) Douglas A. Larson and Jeffrey J. Cronin	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,251,303	10/05/93	Fogg, Jr. et al.	395	275	
	AB	5,432,907	07/11/95	Picazo, Jr. et al.	395	200	
	AC	5,442,770	08/15/95	Barratt	395	403	
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	AT	6,272,609 B1	08/07/01	Jeddeloh	711	169	
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* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

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	BM	6,496,909 B1	12/17/02	Schimmel	711	163	
	BN	6,505,287 B2	01/07/03	Uematsu	711	170	
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	BT	6,622,227 B2	09/16/03	Zumkehr et al.	711	167	
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	BX	2002/0112119 A1	08/15/02	Halbert et al.	711	115	
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	CC							
	CD							
	CE							
	CF							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	CG	Intel, "Intel 840 Chipset: 82840 Memory Controller Hub (MCH)", Datasheet, October 1999, pp. 1-178.
	CH	Micron Technology, Inc., "Synchronous DRAM Module 512MB/1GB (x72, ECC) 168-PIN Registered FBGA SDRAM DIMM", Micron Technology, Inc., 2002, pp. 1-23.
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	CJ	
	CK	
	CL	

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